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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/874,239	06/06/2001	Akira Yamada	57454-132	5917

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EXAMINER	
HO, THANG H	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/874,239	YAMADA, AKIRA	
	Examiner	Art Unit	
	Thang H Ho	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-13 and 15-20* is/are rejected.

7)☒ Claim(s) *7 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy filed on 06/06/2001 has been received.

Information Disclosure Statement

2. The information disclosure statement (IDS) filed on 06/06/2001 has been received and considered. Please see attached PTO-1449.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Specification

4. Claims 1-20 are presented for examination.

5. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is required in correcting any errors of which applicant may become aware in the specification. Appropriate correction is required.

Claim Objections

6. Claims 5-7, 8, 12-14 and 20 are objected to because of the following informalities:

As per claims 5 and 12, the recitation of "a third logic circuit" should be changed to read --a second logic circuit-- or change the dependencies of claims 5 and 12 to depend on claims 3 and 10, respectively.

As per claims 6-7, 13-14 and 20, the recitation of "the said coprocessor" should be changed to read --said coprocessor --.

As per claim 8, on line 13, the recitation of "a logic circuit" should be changed to read --a first logic circuit--.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1-4, 6, 8-11, 13 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Freerksen et al. (United States Patent 6,557,084), hereinafter Freerksen.

As per claim 1, Freerksen discloses a synchronous signal producing **circuit [FIG. 1, bus controller 128]** for synchronizing access by a processor **[FIG. 1, Processor 120]** and a coprocessor **[FIG. 1, Processor 110]** to a shared memory **[FIG. 1, Main**

Memory$_{1-K}$ 130-135, (column 3, lines 61-65)], comprising: an access inhibit region register for designating an access inhibit region for the processor in the shared memory; a comparing circuit for detecting the access by the processor to the access inhibit region designated in the access inhibit region register; and a first logic circuit for issuing a signal setting the processor to a wait state based on a signal indicating that the coprocessor is executing a coprocessor instruction as well as a result of the comparison by the comparing circuit **[Freerksen's synchronous signal producing circuit detects and prevents the coprocessor from accessing stale data from shared memory putting the processor in a wait/retry state, thus an inhibit region register, a comparison circuit and a first logic circuit are required in order to carry out the specified tasks (column 8, lines 3-26)]**.

As per claim 2, Freerksen discloses that the first logic circuit issues the signal setting the processor to the wait state based on the signal indicating that the coprocessor is executing the coprocessor instruction, the result of the comparison by the comparing circuit and a signal indicating that locking of the shared memory is to be released **[column 8, lines 3-26]**.

As per claim 3, Freerksen discloses that the synchronous signal producing circuit, further comprising: a bus wait counter for counting the number of bus wait cycles **[column 6, lines 59-62]**; and a second logic circuit for issuing a bus error signal to the processor based on the signal indicating that the coprocessor is executing the coprocessor

instruction, the result of the comparison by the comparing circuit and a count value of the bus wait counter **[column 6, line 59 through column 7, line 16]**.

As per claim 4, Freerksen discloses that the synchronous signal producing circuit, further comprising: a first initial value register for setting a wait number at the time when the signal issued by the first logic circuit sets the processor to the wait state; a second initial value register for setting a wait number at the time of normal access by the processor; a selector for selecting the values in the first and second initial value registers based on the signal indicating that the coprocessor is executing the coprocessor instruction as well as the result of the comparison by the comparing circuit; and a bus wait counter for receiving the value selected by the selector, and issuing a bus error signal to the processor when the bus wait counter counts the selected value **[column 6, line 59 through column 7, line 16]**.

As per claim 6, Freerksen discloses that the synchronous signal producing circuit, further comprising: a coprocessor instruction execution flag for holding information indicating that the coprocessor is executing the coprocessor instruction, wherein the first logic circuit issues a signal for setting the processor to the wait state based on the information held in the coprocessor instruction execution flag and the result of the comparison by the comparing circuit **[column 8, lines 3-26]**.

As per claims 8-11 and 13, the claims encompass the same scope of invention as to that of claims 1-4 and 6, the claims are therefore rejected for the same reasons set forth above with respect to claims 1-4 and 6.

As per claims 15-20, the claims encompass the same scope of invention as to that of claims 1-4 and 6, however the claims are drafted as method format rather than apparatus format, the claims are therefore rejected for the same reasons set forth above with respect to claims 1-4 and 6.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Freerksen et al. (United States Patent 6,557,084), hereinafter Freerksen, in view of Yamada (United States Patent 5,495,617).

As per claims 5 and 12, Freerksen teaches the invention substantially as claimed. However, Freerksen fails to teach a logic circuit for issuing a signal setting the processor to a low power consumption mode. Yamada teaches a logic circuit for issuing a signal setting the processor to a low power consumption mode **[standby] [a second instruction**

decoder receiving at least a portion of the instruction applied from the instruction register to the first instruction decoder so as to supply a standby control signal to the execution unit (column 3, lines 13-40)]. Accordingly, it would have been prima facie obvious for one skilled in the art at the time the invention was made to implement the synchronous signal producing circuit as taught by Freerksen and incorporating a logic circuit as taught by Yamada to put the processor in a low power consumption mode while waiting for access to a shared memory location to generate the claimed invention with a reasonable expectation of success. One skilled in the art would have been motivated to do so, because the utilization of a logic circuit causes the waiting processing unit to be placed in standby mode resulting in lower power consumption and dissipation, thereby reducing the power requirement by the overall system allowing designers to develop faster and larger processing unit.

Allowable Subject Matter

11. Claims 7 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

13. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to (703) 872-9306

Hand–delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA. Sixth Floor (Receptionist).

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thang H Ho whose telephone number is 703-305-1888. The examiner can normally be reached on Monday-Friday from 7:00 A.M. - 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Thang Ho
Art Unit 2188
January 9, 2004

Kevin L. Ellis
Primary Examiner